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PATENT
Serial No. 09/632,373

IN THE CLAIMS

For the convenience of the Examiner, all pending claims of the present Application are shown below whether or not an amendment has been made.

Please amend the claims as follows.

1. (Cancelled).
2. (Cancelled).
3. (Cancelled).
4. (Cancelled).
5. (Cancelled).
6. (Cancelled).
7. (Cancelled).
8. (Cancelled).
9. (Cancelled).

10. **(Previously presented)** An apparatus for automatically activating a clock master circuit in a stack of repeaters comprising:

a first repeater including a power state output pin, the power state output pin being configured to be connected to ground when the first repeater is powered on;

a second repeater comprising:

a first on pin having a first on pin logical state, the first on pin logical state being indicative of whether or not the second repeater is configured in the stack of repeaters so that no other repeater occupying a position in the repeater stack that is before the position of the second repeater is powered on;

a voltage source connected to the first on pin, the voltage being present when the second repeater is powered on and not present when the second repeater is powered off; and

a clock master circuit that is enabled when the first on pin logical state indicates that no other repeater occupying a position in the repeater stack that is before the position of the second repeater is powered on; and

a connector connecting the first on pin from the second repeater to the power state output pin of the first repeater;

whereby the clock master circuit in the second repeater is enabled based on whether the first repeater is powered on.

11. **(Previously presented)** An apparatus for automatically activating a clock master circuit in a stack of repeaters comprising:

a first repeater comprising means for indicating whether the first repeater is powered on; and

a second repeater comprising:

means for indicating whether the second repeater is powered on;

means for determining whether or not the second repeater is configured in the stack of repeaters so that no other repeater occupying a position in the repeater stack that is before the position of the second repeater is powered on, the means for determining being responsive to said means for indicating whether the first repeater is powered on and said means for indicating whether the second repeater is powered on; and

means for generating a master clock signal, said means for generating comprising means for enabling said means for generating, said means for enabling being responsive to the means for determining;

whereby the means for generating a master clock signal in the second repeater is enabled based on whether the first repeater is powered on.

12. **(Currently amended)** An apparatus for automatically activating a clock master circuit in a repeater comprising:

a local input connector including a local first on pin having a first on pin logical state, the local first on pin logical state being indicative of whether or not the repeater is configured in a stack of repeaters in a manner indicating that the repeater is not selected to activate the clock master circuit and wherein the local input connector is configured to connect the local first on pin to a remote power state output pin on a remote output connector when the local input connector is connected to the remote output connector;

a voltage source connected to the local first on pin, the voltage being present when the repeater is powered on and not present when the repeater is powered of; and

a clock master circuit having an enable input wherein the enable input is controlled by the first on pin logical state;

whereby the clock master circuit is enabled according to the state of the local first on pin and the local first on pin is pulled by the voltage to a first logical state unless the local first on pin is connected to a remote power state output pin that pulls the local first on pin to a second logical state.

13. (Cancelled).

14. (Previously presented) A method of automatically activating a clock master circuit in a stack of repeaters comprising:

selectively connecting a first on pin in a first repeater to a voltage source when the first repeater is powered on;

connecting the first on pin in the first repeater to a power state output pin in a second repeater wherein the power state output pin is configured to be connected to ground when the second repeater is powered on; and

enabling a clock master circuit having an enable input based on the voltage on the first on pin.

15. (Previously presented) A method of automatically activating a clock master circuit in a stack of Fast Ethernet repeaters comprising:

a step for supplying a voltage to a first on pin in the first repeater when the first repeater is powered on;

a step for connecting the first on pin in the first repeater to ground if a second repeater is powered on; and

a step for enabling a clock master circuit based on the voltage on the first on pin.